On-Focal-Plane Signal Processing for Current-Mode Active Pixel Sensors

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***Abstract*— On-focal-plane signal processing for current-mode active pixel sensors (APS), including fixed pattern noise (FPN) suppression and high-resolution analog-to-digital conversion (ADC), is presented. An FPN suppression circuit that removes the offset current variation between pixels by using a combination of an n-type and a p-type current copier cell is described. The FPN suppression circuit exhibits linear transfer characteristics in the input current range from 0 to 30 μA. On-chip ADC is expected to improve imaging system performance and reliability, while reducing system size, weight, and cost. Operation and performance of a current-mode second-order incremental Δ-Σ A/D converter with column parallel architecture and for high-resolution and medium-slow-speed applications is presented. A 12-bit resolution with $\pm$1.5 LSB accuracy at the conversion rate of 5.6 kHz was obtained. The LSB corresponds to less than twelve signal charges of current-mode 10-μm pixel APS's. Based on the experimental results, a brief description of a possible image sensor with the on-chip signal processing is also described.**

I. Introduction

An active pixel sensor (APS) is defined as a detector array that has at least one active transistor within the pixel unit cell [1]. Conventional CCD and MOS image sensors are regarded as "passive pixel sensors" where the photo-generated signal charge at a photosite is transferred to the output amplifier through its readout channel. In comparison with the passive pixel approach, the APS approach has several advantages. Most of them are derived from in-pixel signal amplification or buffering capability. The amplified signal reduces effective read noise [2], which includes the smear noise. The amplified large signal levels alleviate the design of on-chip integrated driving, timing and signal processing circuits. With the APS approach, a highly integrated image sensor can thus be possible [3].

The current readout scheme with a transimpedance amplifier is inherently advantageous in terms of readout speed, because the fixed video line voltage prevents charge-discharge phenomena, while in the voltage readout scheme the load capacitance on the video line is charged and discharged in every pixel signal readout period.

Current-mode signal processing, instead of the conventional voltage-mode signal processing, seems natural and appropriate for current-mode APS's. Switched current (SI) circuits [4] have gained considerable interest for analog sampled-data processing. Advantages of the SI technique over the voltage-mode technique include low supply voltage, potential for high-speed operation, compatibility with standard CMOS process, and less real-estate.

One drawback of the APS is that it produces a large fixed pattern noise (FPN) caused by the electrical characteristic deviation of the active device at the pixel. An on-chip FPN suppression circuit needs to be implemented. In addition, on-chip ADC is expected to improve imaging system performance and reliability, while reducing system size, weight, and cost.

In this paper, a preliminary study of current-mode on-focal-plane signal processing that includes FPN suppression and high-resolution analog-to-digital conversion (ADC) is reported. In Section II, current-mode active pixel sensors are reviewed. A new on-chip FPN suppression circuit is described in Section III. Rationale for on-chip ADC is described in Section IV, followed by the description of architecture, design and experimental results of a current-mode second-order incremental Δ-Σ A/D converter which is suitable for high-resolution, medium-slow-speed applications. In Section V, a brief description of an image sensor with the on-chip ADC is given, following discussion on scaling issue.

II. Current-Mode Active Pixel Sensors

Current-mode active pixel sensors reported so far include a charge modulation device (CMD) image sensor [5] and a CMOS APS [6]. A CMD pixel, and CMOS APS pixels are shown in Fig. 1(a), (b), and (c), respectively.

The CMD pixel consists of only one CMD which has basically an MOS structure with an annular gate electrode. The image sensor operation such as reset, signal hole integration, readout, anti-blooming are controlled by four-level pulse ϕ_G, with each level corresponding to the operations above. The hole-to-current conversion factor is estimated to be 385 pA/e^+ for a 10-μm pixel. The noise sources include the channel current noise and the dark current shot noise. Since the reset is considered to be complete, no reset noise exists. Estimated read noise is 7.6 nA for the noise band width of 20 MHz.

Fig. 1(b) and (c) is the possible circuit configuration of CMOS pixels. Though each pixel is basically the same as a photodiode (PD) pixel [7] and a photogate (PG) pixel [3] where the output signal of the pixel is the voltage change of the photodiode in PD pixel or the voltage change of the floating diffusion in PG pixel, the output of the pixel is a current.

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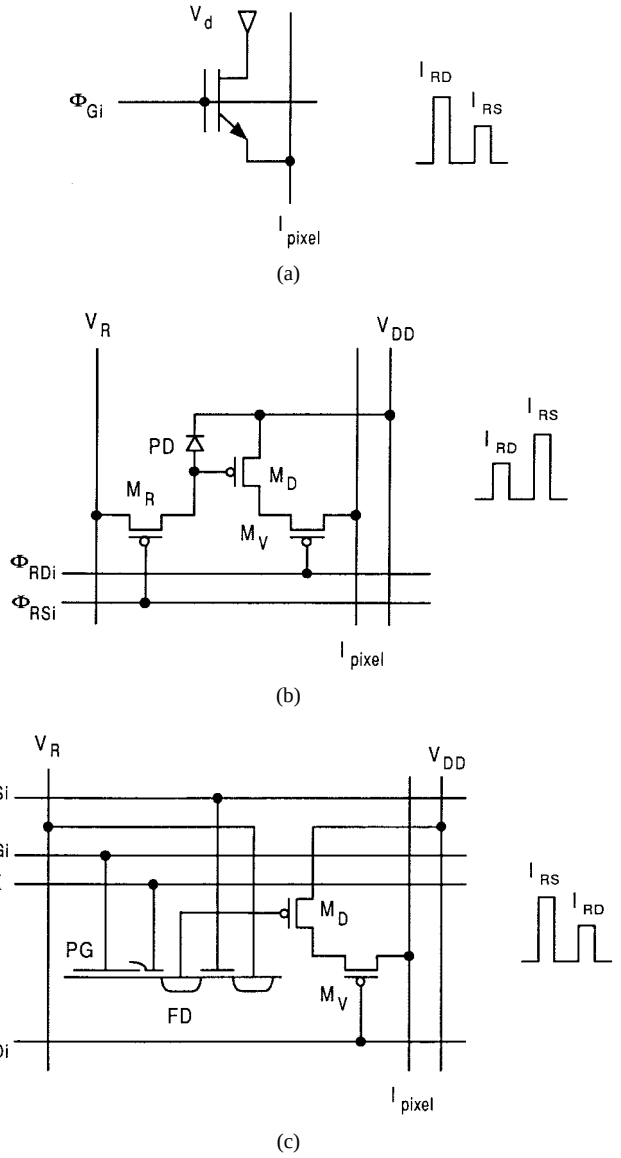

Fig. 1. Pixel configuration of current-mode APS's. (a) CMD pixel. (b) Photodiode (PD) CMOS APS pixel. (c) Photogate (PG) CMOS APS pixel.

In order to couple these pixels directly to a fixed pattern noise (FPN) suppression circuit described in Section III, p-type pixels are employed. However, of course, n-type pixels can be used by changing the polarity of the FPN suppression circuit.

The operation of the PD pixel is as follows. First, the photodiode is reset at the initial voltage V_R by pulsing M_R with the pulse $\phi_{\mathrm{RS}i}$, where i corresponds to the i-th row. During the integration period, photo-induced holes are accumulated at PD, raising the photodiode voltage by $Q_{\mathrm{sig}}/C_{\mathrm{PD}}$, where Q_{sig} is the accumulated charge and C_{PD} is the capacitance associated with the photodiode. During the readout period, when the vertical select switch M_V is turned on by the pulse $\phi_{\mathrm{RD}i}$, the current I_{pixel} flows into the readout circuitry.

In the PG pixel shown in Fig. 1(c), the floating diffusion FD is reset at V_R as the same manner in the PD pixel. During the integration period, the PG being biased at the voltage to form the potential well under PG, photo-induced holes are accumulated under PG. The TX is DC biased at an appropriate value so that excess charge is drained through the FD to the reset drain, which results in high blooming overload protection. Then after the integration period, the PG turns off and the charge is dumped to the floating diffusion FD. During the period when M_V is turned on, the current I_{pixel} which corresponds to the FD voltage is obtained.

FPN, caused by the offset current variations between pixels, can be suppressed as follows. For the PD pixel, the current I_{RD} which consists of the signal current I_{sig} and the offset current I_{off} is first memorized in an FPN suppression circuit. Then the pixels on the selected row are reset and the current I_{RS} which is the offset current I_{off} is memorized. The FPN suppression circuit outputs the difference between I_{RD} and I_{RS}

$$I_{\mathrm{RD}} - I_{\mathrm{RS}} = (I_{\mathrm{sig}} + I_{\mathrm{off}}) - I_{\mathrm{off}} = I_{\mathrm{sig}}. \tag{1}$$

The resultant signal current I_{sig} is FPN-free, in principle.

For the PG pixel, the FD is reset at first and the current I_{RS} is readout. After dumping the signal charge to FD, the current I_{RD} is readout. As in the same manner, FPN suppressed signal current is obtained. With the PG pixel, kTC noise associated with the resetting of FD is also suppressed. The PG pixel is thus superior to the PD pixel in terms of noise performance because the kTC noise cannot be suppressed in the PD pixel because the reset is performed after the signal readout thus the kTC noise in I_{RD} is not correlated with that in I_{RS}. Also it has higher charge-to-current conversion factor because the conversion capacitance is the FD capacitance in the PG pixel while it is the PD capacitance itself in the PD pixel.

From experimental results of voltage-mode 10-μm pixel CMOS APS's [8], the hole-to-current conversion factor is estimated to be 529 pA/e$^-$ for PD pixel and 1850 pA/e$^-$ for PG pixel, respectively. Current noise is come from the channel thermal noise and is estimated to be 8.6 nA for the PD pixel and 4.3 nA for the PG pixel, respectively, for 20 MHz bandwidth.

The signal current is not linear with signal charge. The nonlinear characteristics may not be appropriate for particular applications. This issue will be addressed elsewhere and is beyond the scope of this paper.

III. FPN Suppression

A. Circuit Configuration and Operation

The basic building block of current-mode sampled data circuits is a current copier cell [9] or a dynamic current mirror [10]. The current copier cell operates like a time-multiplexed current mirror that samples an input current on the gate of a MOSFET and outputs a current that is controlled by the same gate voltage, and thus is equal to the input current.

The main performance limitation of a current copier cell is the clock feedthrough associated with the switching MOSFET. There are two mechanisms that cause the clock feedthrough error. The first mechanism is due to transistor channel-charge flow at the timing when transistors turn off. When they turn off, the channel charge must flow out from the channel region of the transistor to the drain and the source junctions, thereby

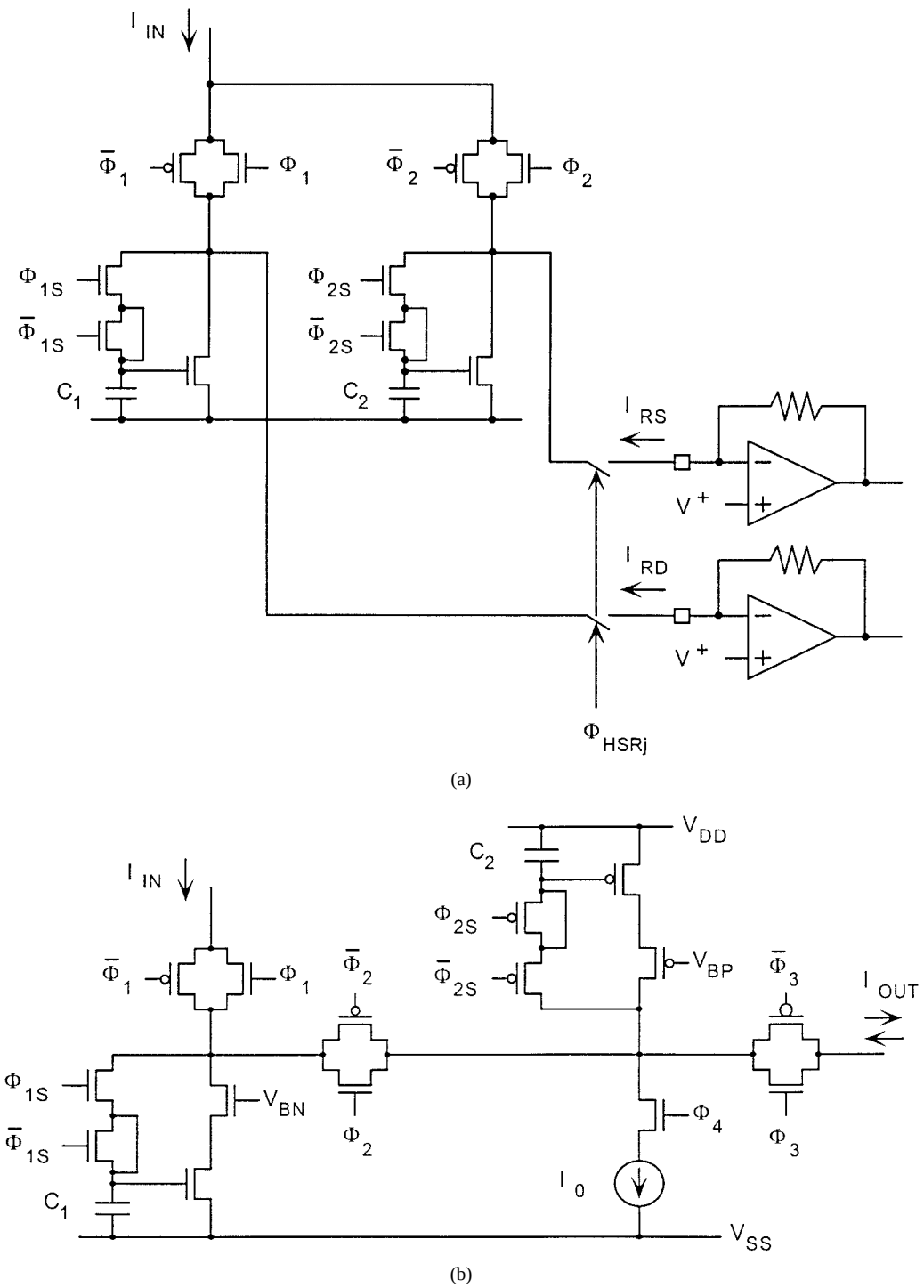

Fig. 2. Current-mode FPN suppression circuits. (a) FPN suppression circuit used in [12]. (b) New FPN suppression circuit.

changing the memorized current. The second one is capacitive coupling between the gate and the source to which a memory capacitor is connected, through overlapping capacitance. The improvement in the clock feedthrough is addressed in Section IV-B-3.

Two types of FPN suppression circuits utilizing current copier cells are shown in Fig. 2. The circuit shown in Fig. 2(a) was used in the CMD image sensor [12]. This circuit is placed for every column at the bottom of the image sensor chip. Its operation is as follows; During the ϕ_1 phase, $I_{\rm RD} = I_{\rm sig} + I_{\rm off}$ is memorized on the first n-channel current copier cell. Then the CMD is reset and during the ϕ_2 phase, $I_{\rm RS} = I_{\rm off}$ is memorized on the second copier cell. These operations are performed during the horizontal blanking period. During the succeeding horizontal scanning period, when the horizontal scanning pulse $\phi_{{\rm HSR}j}$ is applied where j corresponds to the j-th column, two memorized currents are readout simultaneously and an external circuit produces the difference between these two currents. The suppressed FPN of 0.5% for saturation was reported.

A circuit shown in Fig. 2(b) was investigated in this work. Unlike the circuit shown in Fig. 2(a), this circuit employs a single-ended design so that the output current is directly fed to an on-chip analog-to-digital converter described in Section IV and cascode transistors are added to increase the output resistance of the copier. It consists of an n-channel current copier cell and a p-channel current copier cell. Two patterns of pulse timing, shown in Fig. 3 are considered. The pulse timing shown in Fig. 3(a) is applicable for the PG pixel where $I_{\rm RS}$ $(= I_1)$ which is larger than $I_{\rm RD}$ $(= I_2)$ is first readout. During the ϕ_1 phase, $I_1 = I_{\rm off}$ is memorized on the first n-channel current copier cell. Then the signal charge is dumped to the FD. During the ϕ_2 phase, $I_2 = I_{\rm off} - I_{\rm sig}$ is flowing into the circuit, with the first n-channel copier being in the copying (output) phase and the second p-channel copier being in the memorizing (input) phase. The Kirchhoff's current law at the common node for copiers yields the relationship of

$$I_p = I_1 - I_2 + I_0 = I_{\rm sig} + I_0 \tag{2}$$

where I_p is the current memorized on the second copier. The bias current I_0 is added to prevent settling time degradation at the p-copier for small $I_{\rm sig}$. During the ϕ_3 phase, with ϕ_4 on and the p-copier being in the output phase, the FPN suppression circuit outputs $I_{\rm sig}$. This timing is also applicable for the CMD pixel.

The operation of the second timing, shown in Fig. 3(b), is applicable for both the PD and PG pixels. The operation described below is for the PD pixel, while parentheses correspond to the PG pixel. During the ϕ_1 phase, $I_1 = I_{\rm off} - I_{\rm sig}$ $(I_{\rm off})$ is memorized on the first n-channel current copier cell. During the ϕ_2 phase, the pixel is reset and the n-channel copier and the p-channel copier are connected, with the n-copier being in the copying (output) phase and the p-copier being in the memorizing (input) phase. Thus, the p-copier memorizes I_1. Then, ϕ_1 and ϕ_{1S} turn on again, thereby the current $I_2 = I_{\rm off}(I_{\rm off} - I_{\rm sig})$ is memorized on the n-copier. During the ϕ_3 phase when the FPN suppression circuit is connected to its load, both the n- and p-copiers are in the copying (output) phase and the FPN suppression circuit sinks (sources) the current $I_{\rm sig}$. Current I_0 is not needed for this timing.

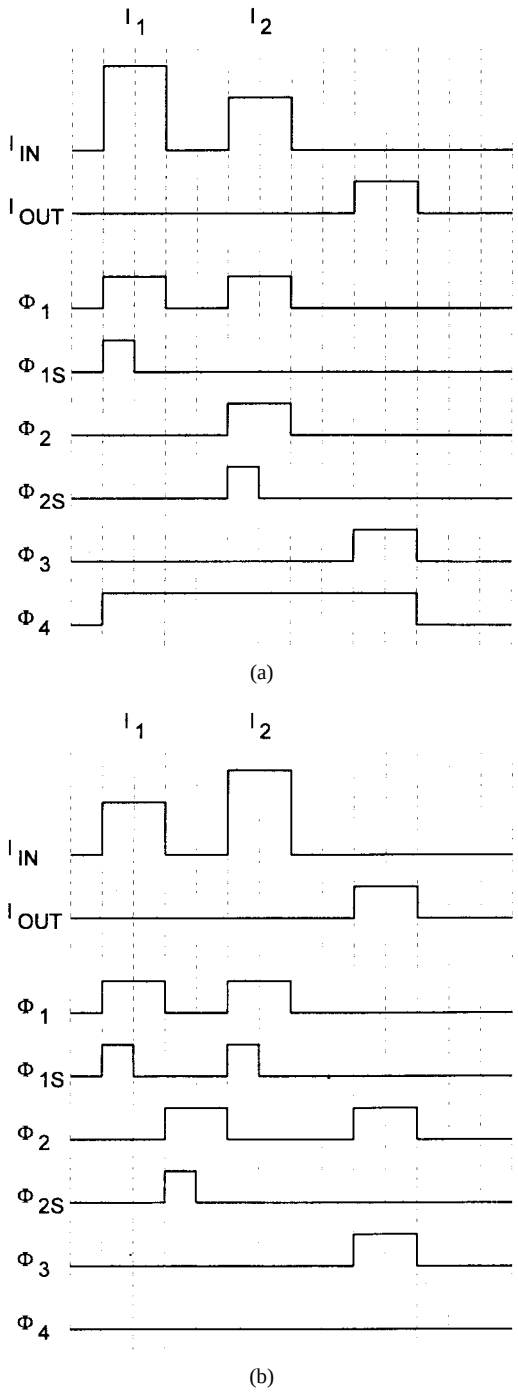

Fig. 3. Pulse timing for the new FPN suppression circuit. (a) Pulse pattern I, applicable for PG pixel and CMD pixel. (b) Pulse timing II, applicable for PD, PG, and CMD pixels.

B. Experimental Results

Fig. 4 shows transfer characteristics obtained with a test element which was fabricated with 2-μm single-poly, double-metal, twin-well CMOS process. The input current denotes the difference between I_1 and I_2 which are shown in Fig. 3. Good linearity with gain of 1.0 was obtained. For the pulse pattern (I) with $I_1 = I_2$ (i.e., the dark situation), the clock feedthrough errors of both the n- and p-copiers contribute to the resulting error. For the pulse pattern (II), only the error of the p-copier contributes, while polarities in PD-mode and PG-mode are opposite. Although the pulse pattern (II) is simpler in operation, noise analysis show that the pulse pattern (I) is expected to yield lower noise than the pulse pattern (II).

The residual FPN will be determined by the variation in the clock feedthrough levels of each FPN suppression circuit thus will be seen as vertical stripes in a reproduced image. To reduce this, the capacitors should be made large within the settling time requirement. It also helps to decrease the detector noise bandwidth.

IV. On-Chip Analog-to-Digital Conversion

A. Rationale for On-Chip ADC

An on-focal-plane analog-to-digital conversion (ADC) is highly desirable to improve imaging system performance and

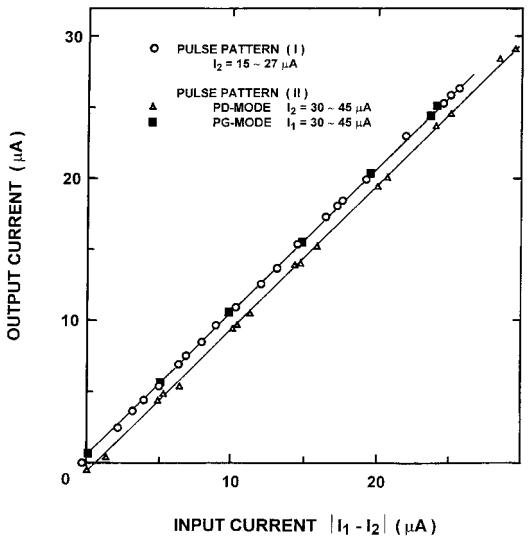

Fig. 4. Transfer characteristics of the FPN suppression circuit.

reliability and to reduce system size, weight, and cost [13]. The approach matches industry trend where A/D conversion is performed as early as possible in a signal chain to avoid analog signal processing and instead utilize digital signal processing, enjoying the benefits of rapidly improving CMOS device technology.

A column parallel approach to analog to digital conversion is considered for implementation of a digital image sensor. In this approach, several ADC's operate in parallel to enable high data rate off the focal plane, while each ADC operates at a lower speed. A bank of ADC's are located at the bottom of the imaging area, where a single ADC may be multiplexed between several columns or may be dedicated to a single column. A column parallel ADC approach leads to reduced power dissipation [13] and noise through the reduction of signal readout bandwidth. Assuming that the main contribution is the white noise, noise in the input signal of an A/D converter is represented by

$$i_n = \sqrt{\int_0^B S_I(f) \cdot df} = \sqrt{S_I(f) \cdot B} \tag{3}$$

where $S_I(f)$ [A^2/Hz] is the output referred noise current power spectrum of a circuit (this may be an FPN suppression circuit described in Section III) prior to an A/D converter and B the analog signal readout bandwidth which may be the bandwidth of an FPN suppression circuit. Since the bandwidth is much smaller in a columnwise ADC than in a serial ADC, column parallel approach is more suitable for low-noise [high-resolution, smaller Least Significant Bit (LSB)] and low-power applications.

B. A Current-Mode Second-Order Incremental Δ-Σ Analog-to-Digital Converter

1) Oversampling A/D Converters: Quantization noise in analog-to-digital conversion can be considered to be white noise distributed from DC to the Nyquist frequency. Thus, it is possible to decrease the quantization noise spectrum by increasing the sampling frequency, since the total noise power is constant. In addition, there are techniques of noise shaping, where most of the quantization noise power is placed outside the signal band and can be removed by low-pass filtering, thus yielding higher signal-to-noise ratio (S/N). Among the techniques, the Δ-Σ modulation [14] is the most popular scheme.

In general, the oversampling converters can be implemented with simple and relatively low precision analog components, while the conventional Nyquist rate converters require high-precision analog circuits. The expense is that fast and complex digital signal processing stages are needed. However, its robustness and the use of fine line width digital CMOS devices are matched with the steadily improving CMOS device technology.

Multiple sampling or oversampling of the detector signal can be much more effectively performed on the focal-plane compared to off-chip [15]. Detector's noise level can be resolved with an on-chip oversampling converter without pre-amplification by simply increasing the oversampling ratio.

2) Architecture: In this work, an on-focal-plane columnwise current-mode Δ-Σ ADC for current-mode active pixel sensors was investigated for high-resolution applications. Compared to the conventional voltage-mode approach which is usually a switched capacitor approach, the current-mode approach is expected to be faster and less sensitive to component variations. The critical elements in switched capacitor approach include linear capacitors and the MOS op-amp which is the slowest analog component and the one most vital to conversion accuracy. The current-mode approach uses no MOS op-amp or linear capacitors. The main building block is again a current copier cell. In order to realize a practical on-chip columnwise ADC, small area and low-power dissipation are required.

A first-order Δ-Σ A/D converter requires 2^n cycles to perform an n-bit ADC. A higher order Δ-Σ, built by incorporating additional error integrator loops, can speed up the conversion. In this work, a cascade of two first-order stages resulting in an incremental Δ-Σ ADC topology was investigated. Since it consists only of cascaded first-order stages, it is immune to loop instabilities. The rationale for choosing a second-order scheme was to avoid large area and power penalties associated with higher order designs, while allowing vastly improved conversion speeds compared to a first order topology.

The architecture of the current-mode second-order incremental Δ-Σ A/D converter is based on the one reported in [16]. Fig. 5 shows a block diagram of the A/D converter. The three main building blocks in the Δ-Σ modulator are the current integrator, current comparator, and the digital-to-analog current converter. There are two loops, connecting in cascade. Output of the comparator "a" for the first comparator and "b" for the second one, becomes "1" if the output of the integrator I is greater than the reference current $I_{\rm ref}$. Otherwise it is "0". A D/A converter in the feedback loop outputs $-I_{\rm ref}$ if the output of the comparator is "1", otherwise it outputs no current.

The detailed operation of the converter based on the block diagram and the pulse timing in Figs. 6 and 7 is as follows

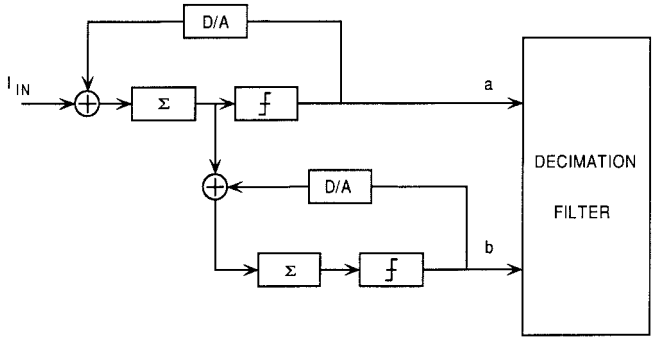

Fig. 5. Block diagram of the second-order incremental A/D converter.

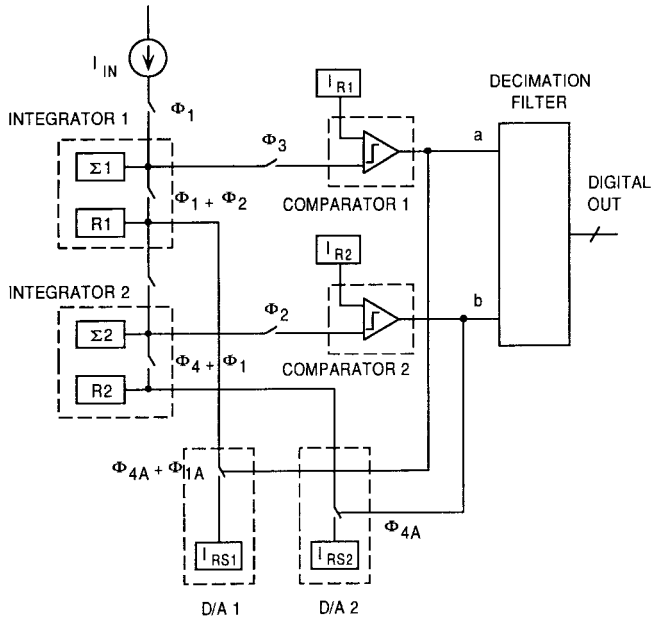

Fig. 6. Block diagram of the current-mode second-order incremental A/D converter.

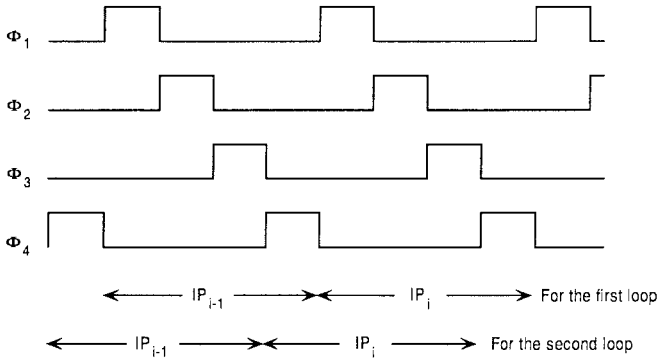

Fig. 7. Pulse timing diagram for the current-mode second-order incremental A/D converter.

[17]. Each integration period consists of four phases. Phase 1 is used to sample the input current. For the first integration period "i" the register $R1$ in the first integrator is zero. Thus, during phase 1 only the input current is memorized at integrator 1's summing current copier $\Sigma 1$. During phase 2, the output of the summer is copied to integrator 1's register. Phase 3 is used to compare the summing current to the reference current I_{R1}. If this copier cell current is greater than the reference, a_1 is a "1". In phase 4, the output current of the integrator 1's register is memorized by integrator 2's summing current copier. If a_1 is a "1", the reference current $I_{\rm RS1}$ is subtracted from the output of the first integrator's register. During the beginning of integration period "$i+1$" starting with phase 1, integrator 1 memorizes the sum of the output of its register and the input current. If a_1 is a "1" the reference current $I_{\rm RS1}$ is also subtracted from this sum.

The timing for the second integrator is the same as the first integrator except the above operations are offset by one phase. During phase 1 (following the phase 4 cycle during which integrator 1's register output was memorized) the current from integrator 2's summing current copier $\Sigma 2$ is copied to integrator 2's register $R2$. During phase 2, the comparison takes place between the summing current copier and the reference current I_{R2}. No events occur during phase 3. During the beginning of the next integration period for the second integrator starting with phase 4, the summing copier memorizes the sum of the output of its register and the output of integrator 1's register. In addition, the reference current $I_{\rm RS2}$ is subtracted if the output of the comparison during phase 2 resulted in b_1 equal to "1".

The expression for two integrator's summing current copier cells to be compared with the reference at the end of "p" integration cycles are

$$I_{\Sigma 1}[p,3] = p \cdot I_{\rm in} - \sum_{i=1}^{p-1} a_i \cdot I_{\rm ref} \tag{4}$$

$$I_{\Sigma 2}[p,2] = \frac{(p-1)\cdot p}{2} \cdot I_{\rm in} - \sum_{i=1}^{p-1} a_i \cdot (p-i) \cdot I_{\rm ref} - \sum_{i=1}^{p-1} b_i \cdot I_{\rm ref}. \tag{5}$$

At the end of p integration cycles the digital representation of the Δ-Σ modulator is determined by

$$DN = \sum_{i=1}^{p-1} a_i \cdot (p-i) + \sum_{i=1}^{p-1} b_i. \tag{6}$$

The digital filter consisting of accumulators is used to generate the digital number. The relationship between resolution of the ADC and the number of integration cycles p (number of times the input current is sampled) is shown in Table I.

3) Implementation: One of limitations in the current copier cell is the charge injection, or the clock feedthrough. An improved current copier cell with an error feedback scheme was reported to yield absolute current error of less than 0.1% [18]. However, its operating speed was slow due to error feedback. A current copier cell named Constant FeedThrough Current Copier Cell (CFTCC), also known as S^2I cell [19], is shown in Fig. 8(a), in which the clock feedthrough is expected to be independent of the input current levels. To compensate charge injection, a dummy switch is employed. Also, a cascode configuration is used to reduce the output conductance effect.

Fig. 8(b) shows a pulse timing diagram for the operation. During the period when the pulses ϕ_1 and ϕ_A are ON, the value $I_{\rm IN}+I_0$ is memorized on C_M. When the pulse is OFF,

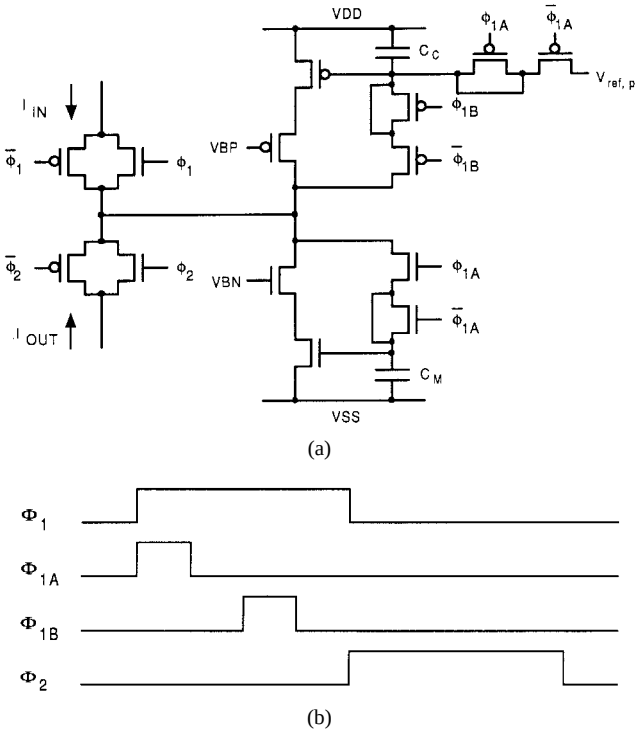

Fig. 8. Constant FeedThrough Current Copier Cell (CFTCCC). (a) Circuit configuration. (b) Pulse timing diagram.

TABLE I
RELATIONSHIP BETWEEN ADC RESOLUTION AND INTEGRATION CYCLES

resolution n (bits)	p
6	12
7	17
8	24
9	33
10	46
11	65
12	92
13	129
14	182

the clock feedthrough corresponding to δI_M, which depends on $I_{\rm IN}$, is added on C_M. Thus, $I_{\rm IN}+I_0+\delta I_M$ is stored on C_M.

During the period when the pulse ϕ_B is ON with ϕ_1 remaining ON, the value $I_0+\delta I_M$ is memorized on C_C. When ϕ_B is OFF, the clock feedthrough corresponding to δI_C, which is constant under the condition of $I_0 \gg \delta I_M$ because of the constant I_0, is added on C_C. Thus, $I_0+\delta I_M+\delta I_C$ is stored on C_C.

During the period when the pulse ϕ_2 is ON, the output current $I_{\rm OUT}$ is obtained. $I_{\rm OUT}$ is given by

$$\begin{aligned} I_{\rm OUT} &= (I_{\rm IN}+I_0+\delta I_M)-(I_0+\delta I_M+\delta I_C) \\ &= I_{\rm IN}-\delta I_C. \end{aligned} \tag{7}$$

Thus, the output current with constant feedthrough can be obtained. The constant offset current results in only the digital number offset in the Δ-Σ A/D converter.

Experimental results of the absolute error (output current-input current) obtained with a test chip are shown in Fig. 9. Data points "a" were obtained with the CFT operation with $I_B = 12.0$ μA, $V_{\rm BP} = 2.25$ V, and $V_{\rm BN} = 2.75$ V. The deviation was almost constant at -270 ± 30 nA in the input current range from 0 to 25 μA. Data points "b" are without cascoding, i.e., $V_{\rm BP} = 0$ V and $V_{\rm BN} = 5$ V. It was confirmed that the cascoding is necessary to obtain desirable performance. Data points "c" are without the CFT operation with cascoding, where no ϕ_{1B} was applied. Although cascoding helps to improve performance, the error is dependent of the input current level.

A current integrator which is a building block of a current-mode Σ-Δ modulator can be built with the CFTCCC's. It consists of an n-channel CFTCCC and a p-channel CFTCCC. The n-channel copier acts as an accumulator and a p-channel copier acts as a temporal register, denoted by Σ and R in Fig. 6, respectively. Prior to the current integration, both two copiers are reset. During the first phase 1, the n-copier is in the memorizing (input) phase while the p-copier is in copying (output) phase. Since the p-copier outputs no current, the n-copier memorizes the input current $I_{\rm IN}$. During the phase 2, the p-copier is in the memorizing phase while the n-copier is in copying phase, thus the p-copier memorizes $I_{\rm IN}$. During the second phase 1, the n-copier memorizes a new $I_{\rm IN}$ from the input terminal and another $I_{\rm IN}$ from the p-copier, thereby memorizing $2I_{\rm IN}$. Current integration continues in this manner.

Fig. 10 shows a current comparator [20]. $I_{\rm ref}$ is provided by the p-channel cascode current source and I flows into an n-channel cascode current sink in the CFTCCC ($\Sigma 1$ or $\Sigma 2$ in Fig. 6). Since the current source and the current sink are connected in series, the smaller current $I_{\rm ref}$ or I flows through the circuit. If I is greater than $I_{\rm ref}$, transistors in the current source operates in the linear region while transistors in the current sink remain in saturation, thereby the input voltage of the comparator becomes "H", yielding the comparator output "H". If I is smaller than $I_{\rm ref}$, the opposite situation occurs and the output of the comparator becomes "L".

As is shown in Fig. 5, each comparator follows an integrating stage. A basic result of this is that the comparator's offset and noise are not as important as in other Nyquist rate A/D configurations where comparators directly measure the analog input.

There are four reference currents, namely I_{R1}, I_{R2}, $I_{\rm RS1}$, and $I_{\rm RS2}$, as shown in Fig. 6. These current sources and sinks are also built with cascoded current copier cells so that these currents can be set to be identical. Reference current set-up operation is performed prior to A-to-D conversion.

4) Performance: The current-mode second-order incremental Δ-Σ modulator was designed and built using 2 μm single-poly, double-metal, twin-well CMOS process. Size of the modulator is 80×1920 μm^2. The digital filter for the test chip was implemented off-chip.

The A/D converter was tested using a computer controlled current source and the output data from the off-chip digital filter was acquired by a computer data acquisition board.

The shortest integration period in Fig. 7 was between 1.28 and 1.92 μs, with the uncertainty resulting from the limited

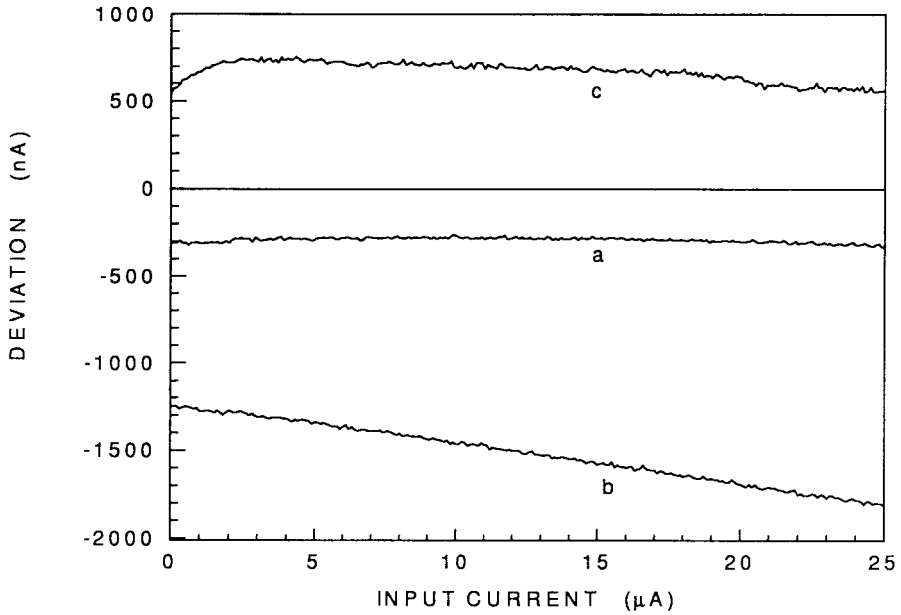

Fig. 9. Absolute error of an n-CFTCCC (a) with CFT operation $V_{\rm BP} = 2.25$ V, $V_{\rm BN} = 2.75$ V, (b) without cascoding $V_{\rm BP} = 0$ V, $V_{\rm BN} = 5$ V, (c) without CFT operation $V_{\rm BP} = 2.25$ V, $V_{\rm BN} = 2.75$ V.

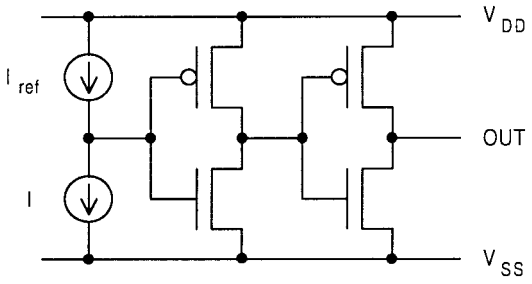

Fig. 10. Current comparator.

time steps supported by the programmable pulse generator used for testing. The conversion time required for particular resolution can be calculated with the number of integration period shown in Table I. With 1.92 μs integration time, the conversion time for 12-bit resolution is 177 μs.

Fig. 11 shows differential nonlinearity (DNL) error for the 12-bit resolution operation. $I_{\rm ref}$ was set at 18.5 μA, thereby 1 LSB corresponding to 4.5 nA. The input current step was 2 nA and 20 samples were acquired at each input step. The DNL error was ± 2 LSB's thus the accuracy of the ADC was ± 1.5 LSB's.

Note that 4.5 nA LSB corresponds to 11.6e$^+$, 8.5e$^+$, and 2.4e$^+$, for a CMD pixel, PD pixel, and PG pixel, respectively.

Fig. 12 shows the measured S/N of the input current. S/N is defined by

$$\frac{S}{N} = 20\log\left(\frac{\langle DN\rangle}{\sigma}\right) \text{(db)} \tag{8}$$

where $\langle DN\rangle$ and σ denote the mean value of the digital number and the standard deviation of 20 samples of the digital number, respectively. The shot noise of the input current was successfully measured. The degradation in S/N seen in the input current range below 80 nA is due to noise coupling from the external measurement circuits.

The DC bias current I_B flows from a p-copier to an n-copier. Since there are four copiers in the modulator, the total DC bias current is $4{\cdot}I_B$. Power dissipation is roughly given by

$$P = V_{\rm DD}\cdot(4I_B + \langle I_1\rangle + \langle I_2\rangle) \tag{9}$$

where I_1 and I_2 denote the current in the first and the second loop of the modulator, respectively, and

$$\langle I_\alpha\rangle = \frac{1}{p}\sum_{i=1}^{p} I_\alpha \quad \alpha = 1, 2. \tag{10}$$

Since the maximum current level is $2\cdot I_{\rm ref}$ for both I_1 and I_2, the maximum signal dependent power dissipation is 360 μW for $I_{\rm ref} = 18$ μA and $V_{\rm DD} = 5$ V. The quiescent power consumption is mainly determined by the bias current I_B. Although an I_B of 40 μA was used in the current implementation, it is possible to operate the ADC with a bias current around 5 μA, if the FPN suppression circuit is used prior to the ADC.

As seen in (9), the power dissipation is dependent of the input signal levels. This is different from a voltage-mode approach, where power dissipation is mainly determined by the bias current of an op-amp. Table II summarizes the performance of the ADC.

V. Discussion and Current-Mode APS with On-Chip Δ-Σ Analog-to-Digital Converter

We consider an image sensor with the on-chip FPN suppression circuits and current-mode second-order incremental Δ-Σ analog-to-digital converters. Fig. 13 shows a block diagram of the image sensor. Each FPN suppression circuit is assigned for each column and its output is fed to an A/D converter.

The A/D converter in a 2 μm design rule occupies approximately 80×5000 μm^2 (0.4 mm^2). In order to realize a practical image sensor, the silicon area of the peripheral

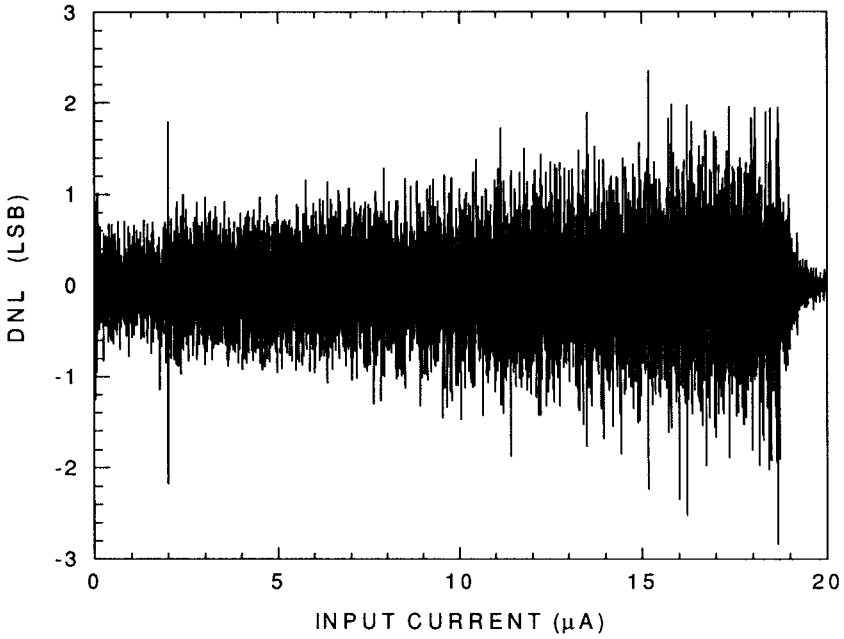

Fig. 11. Differential nonlinearity error for the 12-resolution operation.

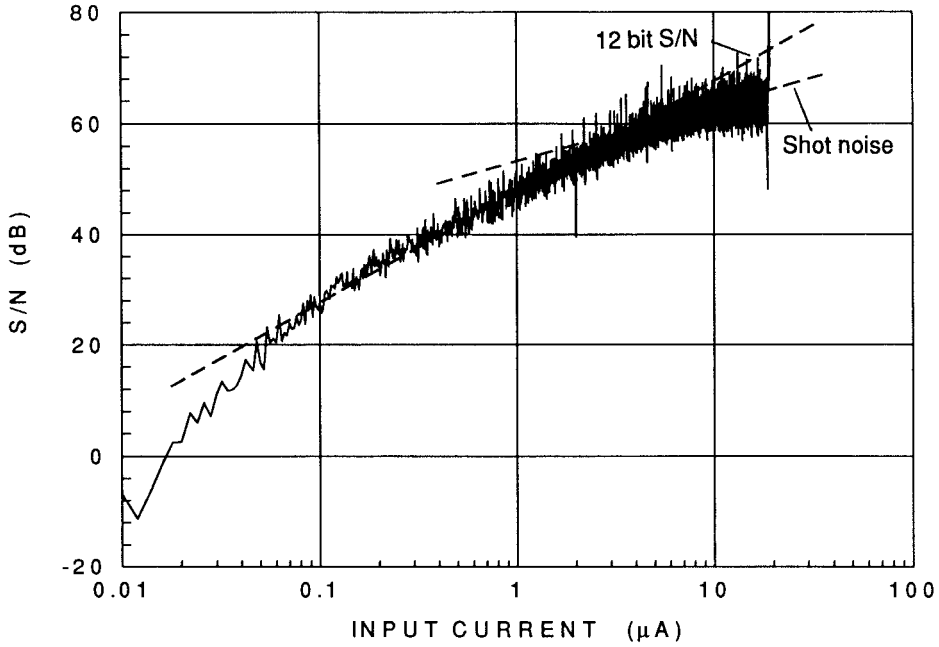

Fig. 12. S/N of the input current.

signal processing circuits as well as scanning circuits should be decreased with scaled CMOS devices. Power supply voltage is also reduced to 3.3 V for CMOS devices of which feature size below 0.5 μm.

Performance of an A/D converter includes accuracy, speed, and power dissipation, and they are expressed as

$$\text{Accuracy} = S/N \propto \frac{V_{\rm GT}}{\sqrt{kT/C}} \tag{11}$$

$$\text{Speed} \propto \frac{g_m}{C} \tag{12}$$

$$\text{power} = V_{\rm DD} \cdot I_D \tag{13}$$

where $V_{\rm GT} = V_{\rm GS} - V_{\rm th}$, and C the holding or load capacitance, respectively.

The operation of the integrator consists of Σ and R as shown in Fig. 6 requires the minimum $V_{\rm DD}$ as

$$\begin{aligned} V_{\rm DD,min} &= 2 \cdot V_{\rm GS,max} - V_{\rm th} + V_{d,\rm sat} \\ &= V_{\rm GS,max} + 2 \cdot V_{d,\rm sat} \end{aligned} \tag{14}$$

where $V_{d,\rm sat}$ is the saturation voltage of a MOSFET. The maximum $V_{\rm GS}$ of the current 2-μm design rule is 2.5 V ($V_{\rm GT} = 1.5$ V and $V_{\rm th} = 1.0$ V) for the maximum handling current of 80 μA in which $I_{\rm sig,max} = 20$ μA and $I_B = 40$ μA. For 0.5-μm design with typical values of $V_{\rm th} = 0.7$ V and

TABLE II
EXPERIMENTAL RESULTS

Supply voltage		V_{DD}=5V V_{SS}=0V
Power dissipation of the modulator		0.8mW quiescent 1.2mW max.
Resolution		12bits
Reference current		18.5μA
I_{LSB}		4.5nA
Conversion time		177μs
Accuracy	Differential nonlinearity	±1.5 LSBs
	Integral nonlinearity	±10 LSBs
Process technology		2μm single poly double metal twin well CMOS
Active area		0.15mm^2

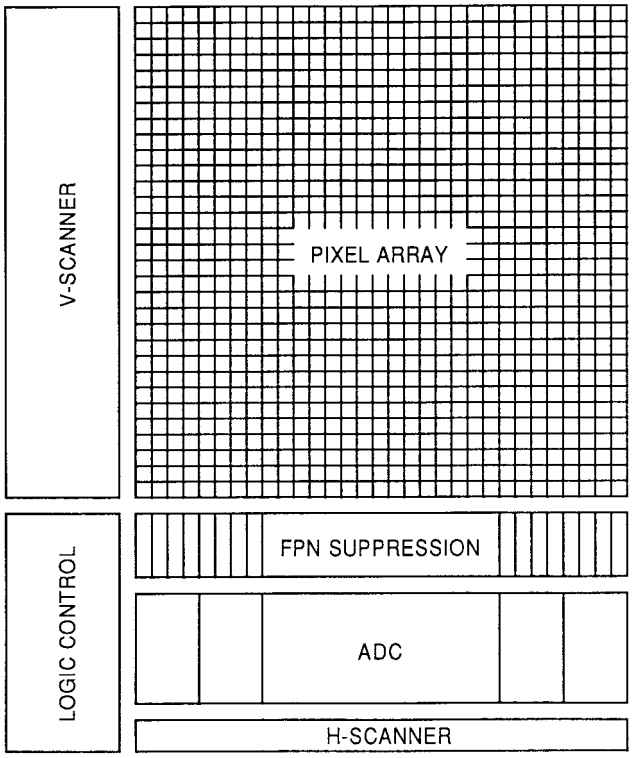

Fig. 13. Block diagram of an image sensor with FPN suppression and analog-to-digital conversion.

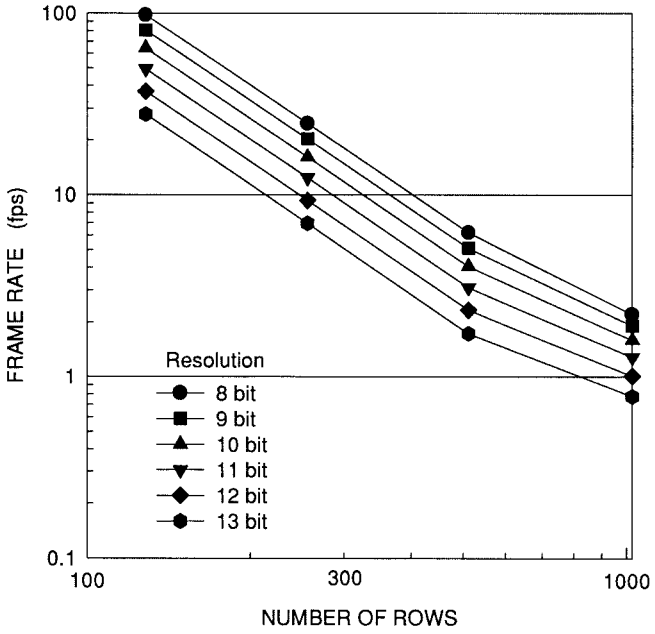

Fig. 14. Estimated relationship between frame rates and the number of rows.

$V_{d,\mathrm{sat}} = 0.1$ V, V_{DD} of 3.3 V is possible with the same V_{GT} from (14). Thus, the dynamic range and accuracy will remain the same from (11), provided the same capacitance value is used. This is unlike voltage mode design, where a reduction of V_{DD} due to technology scaling generally leads to a loss of dynamic range and reduction in operating speed.

With scaling, $K' = \mu \cdot C_{\mathrm{OX}}$ increases

$$K'_s = S_1 \cdot K'_u \quad S_1 > 1 \tag{15}$$

and (W/L) is a design parameter

$$\left(\frac{W}{L}\right)_s = S_2 \cdot \left(\frac{W}{L}\right)_u \tag{16}$$

where subscripts s and u suggest "scaled" and "unscaled" device, respectively. The drain current I_D and the transconductane g_m of an MOS device are given by (assuming square law dependence)

$$I_D = \frac{K' \cdot \left(\frac{W}{L}\right)}{2} \cdot V_{\mathrm{GT}}^2 \tag{17}$$

$$g_m = \sqrt{2K' \cdot \left(\frac{W}{L}\right) \cdot I_D} \tag{18}$$

from (15) to (18)

$$I_{D,s} = S_1 \cdot S_2 \cdot I_{D,u} \tag{19}$$

$$g_{m,s} = S_1 \cdot S_2 \cdot g_{m,u}. \tag{20}$$

If W/L is designed so that $S_1 \cdot S_2 = 1$, both speed and power dissipation remain the same from (12) and (13). However, since the voltage change at the common node of the n-copier (Σ) and the p-copier (R) in the integrator is decreased with the reduced V_{DD}, higher conversion speed is expected. If W/L is designed so that $S_1 \cdot S_2 > 1$ within particular power budget, conversion speed increases. For both cases, reduced clock feedthrough error is expected due to reduced transistor channel charge.

It is estimated from the current layout that the ADC will occupy about 40×2700 μm^2 (0.11 mm^2) silicon area with

standard 0.5 μm design rule, while maintaining the same capacitance value in the analog part. Thus, one ADC can be assigned for every four columns. Fig. 14 shows the estimated relationship between the frame rates and the number of rows. Assumptions include; $N \times N$ pixels, 0.5 μm design rule, the pixel reset time of 2 μs, and reference current set-up operation is performed during the digital data readout period. The figure shows the frame rates in case where one ADC is assigned for every four columns for 1024×1024 pixels, four columns for 512×512 pixels, two columns for 256×256 pixels, and one column for 128×128 pixels, respectively. The pixel size varies accordingly. For a 1×1 k image sensor, chip size and power dissipation are expected to be 12×15 mm^2 and 115 mW.

VI. Conclusion

Current-mode signal processing circuits including a fixed pattern noise (FPN) suppression circuit and a second-order incremental Δ-Σ analog-to-digital converter for current-mode active pixel sensors have been investigated. The FPN suppression circuit implemented with a combination of an n-type and a p-type current copier cell exhibits a linear transfer characteristics in the input current range from 0 to 30 μA, in which offset currents are subtracted from signal currents. A 12-bit resolution with ± 1.5 LSB accuracy at the conversion rate of 5.6 kHz was obtained with the Δ-Σ A/D converter . An LSB is 4.5 nA which corresponds to less than 12 signal charges of current-mode 10-μm pixel APS's. Based on the experimental results, an image sensor with the on-chip ADC, having 1×1 k pixels with pixel size of 10×10 μm^2, is expected to have 12-bit A/D resolution with frame rate of 1.0 frame/s, power dissipation of 115 mW, and the chip size of approximately 12×15 mm^2.

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